embodiments disclosed are within the scope of the invention as encompassed by the following claims.

WE CLAIM:

CLAIMS

1. A method for producing grain boundary-free polycrystalline silicon, the method comprising:

forming a film of amorphous silicon;

using a 2N-shot laser irradiation process to form polycrystalline silicon in a first area of the film;

selecting a second area, included in the first area; and,

using a directional solidification (DS) process to anneal the second area.

2. The method of claim 1 wherein using a 2N-shot laser irradiation process to form polycrystalline silicon in a first area of the film includes sequencing irradiation in odd and even iteration patterns, the patterns including:

for odd numbered iterations, projecting a first laser beam, in two steps, through a first aperture pattern oriented in a first direction; and,

for even numbered iterations, projecting the first laser beam, in two steps, through a second aperture pattern oriented in a second direction orthogonal to the first direction.

3. The method of claim 2 wherein using a 2N-shot laser irradiation process to form polycrystalline silicon in a first area of the film includes forming in the first area:

a first plurality of parallel grain boundaries oriented in the first direction and having consecutive grain boundaries equally spaced by a first width; and,

a second plurality of parallel grain boundaries oriented in the second direction and having consecutive grain boundaries equally spaced by a second width.

4. The method of claim 3 wherein forming first and second pluralities of grain boundaries having respective consecutive grain boundaries equally spaced by first and second widths, respectively, includes:

selecting the first width in a range of 0.1 microns (μm) to 100 μm; and,

selecting the second width in a range of 0.1 μm to 100 μm.

5. The method of claim 4 wherein selecting the first and second widths in respective ranges of 0.1 μm to 100 μm includes:

selecting the first width in a range of 0.1 μm to 0.6 μm; and,

selecting the second width in a range of 0.1 μm to 0.6 μm.

6. The method of claim 5 wherein selecting the first and second widths in respective ranges of 0.1 μm to 0.6 μm includes:

selecting the first width in a range of 0.3 μm to 0.6 μm; and,

selecting the second width in a range of 0.3 μm to 0.6 μm.

7. The method of claim 4 wherein selecting the first and second widths in respective ranges of 0.1 μm to 100 μm includes:

selecting the first width in a range of 0.6 μm to 10 μm; and,

selecting the second width in a range of 0.6 μm to 10 μm.

8. The method of claim 4 wherein selecting the first and second widths in respective ranges of 0.1 μm to 100 μm includes:

selecting the first width in a range of 10 μm to 100 μm; and,

selecting the second width in a range of 10 μm to 100 μm.

9. The method of claim 3 wherein forming first and second pluralities of grain boundaries with first and second widths, respectively, includes selecting the first and second widths to be equal.

10. The method of claim 3 wherein sequencing irradiation in odd and even iteration patterns includes performing one odd iteration and one even iteration.

11. The method of claim 3 wherein using a DS process to anneal the second area includes:

selecting a third aperture pattern;

orienting the third aperture pattern and a second area top surface in the first direction;

projecting a second laser beam through the third aperture pattern to anneal a first portion of the second area;

sequentially:

advancing the third aperture pattern and the second area top surface in the first direction;

projecting the second laser beam through the third aperture pattern; and,

annealing remaining portions of the second area; and,

selectively removing grain boundaries in the second area.

12. The method of claim 11 wherein selectively removing grain boundaries in the second area includes:

smoothing ridges formed by the first and second pluralities of grain boundaries; and,

removing grain boundaries with the exception of first plurality grain boundaries.

13. The method of claim 12 wherein selecting the second area includes:

selecting a first pair of sides parallel to and located between first plurality grain boundaries; and,

selecting a second pair of sides parallel to and located between second plurality grain boundaries.

14. The method of claim 13 wherein selecting a first pair of sides located between first plurality grain boundaries includes selecting at least one first pair side to be co-located on a first plurality grain boundary.

15. The method of claim 13 wherein selecting a first pair of sides located between first plurality grain boundaries includes selecting a first pair of sides located between consecutive first plurality grain boundaries.

16. The method of claim 15 wherein selecting a first pair of sides located between consecutive first plurality grain boundaries

includes selecting at least one first pair side to be co-located on a consecutive first plurality grain boundary.

17. The method of claim 13 wherein selecting a second pair of sides located between second plurality grain boundaries includes selecting at least one second pair side to be co-located on a second plurality grain boundary.

18. The method of claim 11 wherein orienting the third aperture pattern and a second area top surface in the first direction includes selecting the first direction the same as a direction of a last iteration in a 2N-shot iteration sequence performed on the first area.

19. The method of claim 3 wherein projecting a first laser beam through first and second aperture patterns includes using a first excimer laser source with a wavelength between 248 nanometers (nm) and 308 nm to supply the first laser beam; and,

wherein projecting a second laser beam through a third aperture pattern includes using a second excimer laser source with a wavelength between 248 nm and 308 nm to supply the second laser beam.

20. The method of claim 3 wherein projecting a first laser beam through first and second aperture patterns includes projecting the first laser beam for a pulse duration of up to 300 nanoseconds (ns); and,

wherein projecting a second laser beam through a third aperture pattern includes projecting the second laser beam for a pulse duration of up to 300 ns.

21. The method of claim 20 wherein projecting a first laser beam through first and second aperture patterns includes projecting the first laser beam for a pulse duration of up to 30 ns.

22. The method of claim 3 wherein projecting a first laser beam through first and second aperture patterns includes projecting the first laser beam by a factor of one.

23. The method of claim 20 wherein projecting the second laser beam through the third aperture pattern includes projecting the second laser beam for a pulse duration of up to 30 ns.

24. The method of claim 11 wherein projecting a second laser beam through the third aperture pattern includes projecting the second laser beam by a factor of one.

25. The method of claim 3 wherein projecting a first laser beam to anneal the first area includes exposing the first area to a first energy density from the first laser beam;

the method further comprising:

projecting a third laser beam onto the first area; and,

exposing the first area to a second energy density from the third laser beam; and,

wherein annealing the first area includes:

summing the first and second energy densities to yield a third energy density; and,

annealing the first area in response to the third energy density.

26. The method of claim 25 wherein projecting a third laser beam onto the first area includes projecting, from a solid state laser source, a third laser beam with a wavelength of 532 nm and a pulse duration of between 50 ns and 150 ns.

27. The method of claim 25 wherein projecting a third laser beam onto the first area includes projecting, from a carbon dioxide (CO_2) laser source, a third laser beam with a wavelength in a range of 10.2 μm to 10.8 μm and a pulse duration of up to 4 milliseconds (ms).

28. The method of claim 3 wherein projecting a first laser beam to anneal the first area includes exposing the first area to a fourth energy density from the first laser beam;

the method further comprising:

exposing the first area to a first lamp light; and

exposing the first area to a fifth energy density from the first lamp light; and,

wherein annealing the first area includes:

summing the fourth and fifth energy densities to yield a sixth energy density; and,

annealing the first area in response to the sixth energy density.

29. The method of claim 28 wherein exposing the first area to a first lamp light includes exposing the first area to light from an excimer lamp with a wavelength less than 550 nm.

30. The method of claim 28 wherein exposing the first area to a first lamp light includes exposing a first bottom surface of the amorphous silicon film including the first area.

31. The method of claim 28 wherein exposing the first area to a first lamp light includes exposing a first top surface of the amorphous silicon film including the first area.

32. The method of claim 11 wherein projecting a second laser beam to anneal the second area includes exposing the second area to a seventh energy density from the second laser beam;

the method further comprising:

projecting a fourth laser beam onto the second area; and,

exposing the second area to an eighth energy density from the fourth laser beam; and,

wherein annealing the second area includes:

summing the seventh and eighth energy densities to yield a ninth energy density; and,

annealing the second area in response to the ninth energy density.

33. The method of claim 32 wherein projecting a fourth laser beam onto the second area includes projecting, from a solid state laser source, a fourth laser beam with a wavelength of 532 nm and a pulse duration of between 50 ns and 150 ns.

34. The method of claim 32 wherein projecting a fourth laser beam onto the second area includes projecting, from a CO_2 laser source, a third laser beam with a wavelength in a range of 10.2 μm to 10.8 μm and a pulse duration of up to 4 ms.

35. The method of claim 11 wherein projecting a second laser beam to anneal the second area includes exposing the second area to a tenth energy density from the second laser beam;

the method further comprising:

exposing the second area to a second lamp light; and

exposing the second area to an eleventh energy density from the second lamp light; and,

wherein annealing the second area includes:

summing the tenth and eleventh energy densities to yield a twelfth energy density; and,

annealing the second area in response to the twelfth energy density.

36. The method of claim 35 wherein exposing the second area to a second lamp light includes exposing the second area to light from an excimer lamp with a wavelength less than 550 nm.

37. The method of claim 35 wherein exposing the second area to a second lamp light includes exposing a second bottom surface of the amorphous silicon film including the second area.

38. The method of claim 35 wherein exposing the second area to a second lamp light includes exposing a second top surface of the amorphous silicon film including the second area.

39. The method of claim 11 further comprising:

forming a transparent substrate layer;

forming a diffusion barrier overlying the substrate layer and underlying the first area;

forming in the second area, a transistor channel with a length, oriented in the first direction, and a width;

forming in the first area, source and drain regions adjacent to the channel region;

forming a gate dielectric layer overlying the transistor channel, source, and drain regions, the dielectric thickness in a range of 20 angstroms (A) to 500 A over the channel region; and,

forming a gate electrode overlying the gate dielectric layer.

40. The method of claim 39 wherein forming a channel region with a length includes forming the channel length with a first pair of sides parallel to and located between a pair of first plurality grain boundaries; and,

wherein forming a channel region with a width includes forming the channel width with a second pair of sides parallel to and located between a pair of second plurality grain boundaries.

41. The method of claim 40 wherein forming the channel length with a first pair of parallel sides located between a pair of first plurality grain boundaries includes co-locating at least one side from the first pair on a first plurality grain boundary.

42. The method of claim 40 wherein forming the channel length with a first pair of parallel sides located between a pair of first plurality grain boundaries includes forming the channel length with a first pair of parallel sides located between a pair of consecutive first plurality grain boundaries.

43. The method of claim 42 wherein forming the channel length with a first pair of parallel sides located between a pair of consecutive first plurality grain boundaries includes co-locating at least one side from the first pair on a first plurality grain boundary.

44. The method of claim 40 wherein forming the channel width with a second pair of parallel sides located between a pair of second plurality grain boundaries includes co-locating at least one side from the second pair on a second plurality grain boundary.

45. The method of claim 40 wherein forming first and second pluralities of grain boundaries having respective consecutive grain

boundaries equally spaced by first and second widths, respectively, includes:

selecting the first width in a range of 0.1 μm to 100 μm; and,

selecting the second width in a range of 0.1 μm to 100 μm.

46. The method of claim 45 wherein selecting the first width in a range of 0.1 μm to 100 μm includes selecting the first width in a range of 0.3 μm to 0.6 μm; and,

wherein forming a transistor channel includes:

for n-type TFTs, forming the channel with a carrier mobility of greater than 500 square centimeters per volt-second (cm^2/Vs) and a threshold voltage (V_{th}) of less than and equal to +/- 0.35V in a range of 0V to 1V; and,

for p-type TFTs, forming the channel with an carrier mobility of greater than 200 cm^2/Vs and a V_{th} of less than and equal to +/- 0.35V in a range of -1V to 0V.

47. The method of claim 45 wherein selecting the first width in a range of 0.1 μm to 100 μm includes selecting the first width in a range of 0.6 μm to 10 μm; and,

wherein forming a transistor channel includes:

for n-type TFTs, forming the channel with an carrier mobility of greater than 700 cm^2/Vs and a V_{th} of less than and equal to +/- 0.1V in a range of 0V to 0.8V; and,

for p-type TFTs, forming the channel with an carrier mobility of greater than 250 cm^2/Vs and a V_{th} of less than and equal to +/- 0.1V in a range of -0.8V to 0V.

48. The method of claim 45 wherein selecting the first width in a range of 0.1 μm to 100 μm includes selecting the first width in a range of 10 μm to 100 μm; and,

wherein forming a transistor channel includes:

for n-type TFTs, forming the channel with an carrier mobility of approximately 750 cm^2/Vs and a V_{th} of less than and equal to +/- 0.01V in a range of 0V to 0.1V; and,

for p-type TFTs, forming the channel with an carrier mobility of greater than 250 cm^2/Vs and a V_{th} of less than and equal to +/- 0.01V in a range of -0.1V to 0V.

49. A polycrystalline silicon film with a quasi-single crystal region, the film comprising:

a polycrystalline grid region having a first plurality of parallel grain boundaries orthogonal to a second plurality of parallel grain boundaries; and,

in the grid region, a third plurality of quasi-single crystals, each crystal having:

a first pair of sides forming a length, the first pair of sides parallel to and located between a pair of consecutive first plurality grain boundaries; and,

a second pair of sides forming a width, the second pair of sides parallel to and located between a pair of second plurality grain boundaries.

50. The film of claim 49 wherein at least one side in the first pair of sides is co-located on a first plurality grain boundary.

51. The film of claim 49 wherein at least one side in the second pair of sides is co-located on a second plurality grain boundary.

52. The film of claim 49 wherein the third plurality of quasi-single crystals includes crystals with shared grain boundaries.

53. The film of claim 49 wherein grid region first plurality consecutive grain boundaries are equally separated by a first distance in a range of 0.1 microns (μm) to 100 μm; and,

wherein grid region second plurality consecutive grain boundaries are equally separated by a second distance in a range of 0.1 μm to 100 μm.

54. The film of claim 53 wherein grid region first plurality consecutive grain boundaries are equally separated by a first distance in a range of 0.3 μm to 0.6 μm;

wherein for n-type film, the carrier mobility is greater than 500 square centimeters per volt-second (cm^2/Vs); and,

wherein for p-type film, the carrier mobility is greater than 200 cm^2/Vs.

55. The film of claim 53 wherein grid region first plurality consecutive grain boundaries are equally separated by a first distance in a range of 0.6 μm to 10 μm;

wherein for n-type film, the carrier mobility is greater than 700 cm^2/Vs; and,

wherein for p-type film, the carrier mobility is greater than 250 cm^2/Vs.

56. The film of claim 53 wherein grid region first plurality consecutive grain boundaries are equally separated by a first distance in a range of 10 μm to 100 μm;

wherein for n-type film, the carrier mobility is approximately 750 cm^2/Vs; and,

wherein for p-type film, the carrier mobility is greater than 250 cm^2/Vs.

57. A thin film transistor (TFT) with a channel region formed from quasi-single crystal silicon, the TFT comprising:

a transparent substrate;

a diffusion barrier overlying the transparent substrate;

a polycrystalline silicon grid region, overlying the diffusion barrier, the grid region including:

a first plurality of parallel grain boundaries orthogonal to a second plurality of parallel grain boundaries;

a channel region formed from a plurality of quasi-single crystals having shared grain boundaries, each crystal having:

a first pair of sides forming a length, the first pair of sides parallel to and located between a pair of consecutive first plurality grain boundaries; and,

a second pair of sides forming a width, the second pair of sides parallel to and located between a pair of second plurality grain boundaries;

source and drain regions adjacent the channel region;

an oxide gate insulator layer overlying the silicon layer, the insulator layer having a thickness in a range of 20 angstroms (A) to 500 A over the channel region; and,

a gate electrode overlying the oxide gate insulator layer.

58. The TFT of claim 57 wherein at least one side in the first pair of sides is co-located on a first plurality grain boundary.

59. The TFT of claim 57 wherein at least one side in the second pair of sides is co-located on a second plurality grain boundary.

60. The TFT of claim 57 wherein the channel region is formed from a single quasi-single crystal.

61. The TFT of claim 57 wherein grid region first plurality consecutive grain boundaries are equally separated by a first distance in a range of greater than 0.1 microns (μm) to 100 μm; and,

wherein grid region second plurality consecutive grain boundaries are equally separated by a second distance in a range of greater than 0.1 μm to 100 μm.

62. The TFT of claim 61 wherein grid region first plurality consecutive grain boundaries are equally separated by a first distance in a range of 0.3 μm to 0.6 μm; and,

wherein the channel region has:

for n-type TFTs, an carrier mobility of greater than 500 square centimeters per volt-second (cm^2/Vs) and a threshold voltage (V_{th}) of less than and equal to +/- 0.35V in a range of 0V to 1V; and,

for p-type TFTs, an carrier mobility of greater than 200 cm^2/Vs and a V_{th} of less than and equal to +/- 0.35V in a range of -1V to 0V.

63. The TFT of claim 61 wherein grid region first plurality consecutive grain boundaries are equally separated by a first distance in a range of 0.6 μm to 10 μm; and,

wherein the channel region has:

for n-type TFTs, an carrier mobility of greater than 700 cm^2/Vs and a V_{th} of less than and equal to +/- 0.1V in a range of 0V to 0.8V; and,

for p-type TFTs, an carrier mobility of greater than 250 cm^2/Vs and a V_{th} of less than and equal to +/- 0.1V in a range of -0.8V to 0V.

64. The TFT of claim 61 wherein grid region first plurality grain boundaries are equally separated by a first distance in a range of 10 μm to 100 μm; and,

wherein the channel region has:

for n-type TFTs, an carrier mobility of approximately 750 cm^2/Vs and a V_{th} of less than and equal to +/- 0.01V in a range of 0V to 0.1V; and,

for p-type TFTs, an carrier mobility of greater than 250 cm^2/Vs and a V_{th} of less than and equal to +/- 0.01V in a range of -0.1V to 0V.